CVE-2025-35979

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Summary

CVE	CVE-2025-35979
State	PUBLISHED
Assigner	intel
Source Priority	CVE Program / NVD first with legacy fallback
Published	2026-05-12 17:16:13 UTC
Updated	2026-05-13 15:52:56 UTC
Description	Exposure of sensitive information caused by shared microarchitectural predictor state that influences transient execution fo

Risk And Classification

Primary CVSS: v4.0 6.8 MEDIUM from secure@intel.com

CVSS:4.0/AV:L/AC:H/AT:P/PR:L/UI:N/VC:H/VI:N/VA:N/SC:H/SI:N/SA:N/E:X/CR:X/IR:X/AR:X/MAV:X/MAC:X/MAT:X/MPR:X/MUI:X/MVC:X/MVI:X/MVA:X/MSC:X/MSI:X/MSA:X/S:X/AU:X/R:X/V:X/RE:X/U:X

EPSS: 0.000150000 probability, percentile 0.031500000 (date 2026-05-13)

Problem Types: Information Disclosure | CWE-1423 Exposure of Sensitive Information caused by Shared Microarchitectural Predictor State that Influences Transient Execution

Version	Source	Type	Score	Severity	Vector
4.0	secure@intel.com	Secondary	6.8	MEDIUM	CVSS:4.0/AV:L/AC:H/AT:P/PR:L/UI:N/VC:H/VI:N/VA:N/SC:H/SI:N/SA:N/E:X/C.
4.0	CNA	CVSS	6.8	MEDIUM	CVSS:4.0/AV:L/AC:H/AT:P/PR:L/UI:N/VC:H/VI:N/VA:N/SC:H/SI:N/SA:N

CVSS v4.0 Breakdown

Attack Vector

Local

Attack Complexity

High

Attack Requirements

Present

Privileges Required

Low

User Interaction

None

Confidentiality

High

ntegrity

None

Availability

None

Sub Conf.

High

Sub Integrity

None

Sub Availability

None

CVSS:4.0/AV:L/AC:H/AT:P/PR:L/UI:N/VC:H/VI:N/VA:N/SC:H/SI:N/SA:N/E:X/CR:X/IR:X/AR:X/MAV:X/MAC:X/MAT:X/MPR:X/MUI:X/MVC:X/MVI:X/MVA:X/MSC:X/MSI:X/MSA:X/S:X/AU:X/R:X/V:X/RE:X/U:X

Vendor Declared Affected Products

Source	Vendor	Product	Version	Platforms
CNA	Na	IntelR Processors	affected See references	Not specified

References

Reference	Source	Link	Tags
intel.com/content/www/us/en/security-center/advisory/intel-sa-01420.html	secure@intel.com	intel.com	
CVE Program record	CVE.ORG	www.cve.org	canonical
NVD vulnerability detail	NVD	nvd.nist.gov	canonical, analysis

No vendor comments have been submitted for this CVE.

There are currently no legacy QID mappings associated with this CVE.

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